CLAIMS

What is claimed is:

1. An apparatus for compensating for glitch occurrence in a reset signal that is applied in an integrated circuit, the apparatus comprising:

a logic stage capable to process an incoming signal and a delayed incoming signal that is a delayed version of the incoming signal, the logic stage capable to generate an output signal so that when the incoming signal and the delayed incoming signal are in the same state, the output signal will be in the same state.

2. The apparatus of claim 1 wherein the logic stage comprises an S-R flip flop.

3. The apparatus of claim 1 wherein the logic stage comprises:

a NAND gate capable to receive the incoming signal and the delayed incoming signal;

a NOR gate capable to receive the incoming signal and the delayed incoming signal; and

an inverter communicatively coupled to the NOR gate and capable to invert an output NOR gate signal from the NOR gate.

4. The apparatus of claim 1 wherein the logic stage comprises:

a NAND gate capable to receive the incoming signal and the delayed incoming signal; and

an OR gate capable to receive the incoming signal and the delayed incoming signal.

5. The apparatus of claim 1 wherein the delayed incoming signal is delayed by a delay stage.

6. The apparatus of claim 1 wherein the logic portion is capable to filter at least one of a first glitch occurring before a high state portion of the incoming signal and a second glitch occurring after the high state portion of the incoming signal.

7. A method of compensating for a glitch in an incoming signal used for resetting an integrated circuit, the method comprising:

receiving an incoming signal;

delaying a glitch occurrence in an incoming signal into a delayed incoming signal;

performing a logic operation on the incoming signal and the delayed incoming signal; and

generating an output signal so that when the incoming signal and the delayed incoming signal are in the same state, the output signal will be in the same state.

8. The method of claim 7, further comprising:

applying the generated output signal as a reset signal to at least some portion of an integrated circuit.

9. The method of claim 7 wherein the generating the output signal comprises:

filtering at least one of a first glitch occurring before a high state portion of the incoming signal and a second glitch occurring after the high state portion of the incoming signal.

10. An apparatus for compensating for glitch occurrence in a reset signal that is applied in an integrated circuit, the apparatus comprising:

a logic stage capable to process an incoming signal and a delayed incoming signal that is a delayed version of the incoming signal, the logic stage capable to generate an output signal so that when the incoming signal and the delayed incoming signal are in the same state, the output signal will have a state similar to the state of the incoming signal, and when the incoming signal and the delayed incoming signal are not in the same state, the output signal will have a state similar to a previously sampled state of the incoming signal.

11. The apparatus of claim 10 wherein the logic stage comprises:

an exclusive NOR gate; and

a pass-through circuit communicatively coupled to the exclusive NOR gate and capable to pass through the incoming signal in response to an output value from the exclusive NOR gate.

12. The apparatus of claim 10 wherein the delayed incoming signal is delayed by a delay stage.

13. The apparatus of claim 10 wherein the logic portion is capable to filter at least one of a first glitch occurring before a high state portion of the incoming signal and a second glitch occurring after the high state portion of the incoming signal.

14. A method of compensating for a glitch in an incoming signal used for resetting an integrated circuit, the method comprising:

receiving an incoming signal;

delaying a glitch occurrence in an incoming signal into a delayed incoming signal;

performing a logic operation on the incoming signal and the delayed incoming signal; and

generating an output signal so that when the incoming signal and the delayed incoming signal are in the same state, the output signal will have a state similar to the state of the incoming signal, and when the incoming signal and the delayed incoming signal are not in the same state, the output signal will have a state similar to a previously sampled state of the incoming signal.

15. The method of claim 14, further comprising:

applying the generated output signal as a reset signal to at least some portion of an integrated circuit.

16. The method of claim 14 wherein the generating the output signal comprises:

filtering at least one of a first glitch occurring before a high state portion of the incoming signal and a second glitch occurring after the high state portion of the incoming signal.